TPA3251 175-W Stereo, 350-W Mono PurePath™ Ultra-HD Analog-Input Class-D Amplifier

1 Features

- Differential Analog Inputs
- Total Output Power at 10%THD+N
  - 175-W Stereo into 4 Ω in BTL Configuration
  - 220-W Stereo into 3 Ω in BTL Configuration
  - 350-W Mono into 2 Ω in PBTL Configuration
- Total Output Power at 1%THD+N
  - 140-W Stereo into 4 Ω in BTL Configuration
  - 175-W Stereo into 3 Ω in BTL Configuration
  - 285-W Mono into 2 Ω in PBTL Configuration
- Advanced Integrated Feedback Design with High-speed Gate Driver Error Correction (PurePath™ Ultra-HD)
  - Signal Bandwidth up to 100 kHz for High Frequency Content From HD Sources
  - Ultra Low 0.005% THD+N at 1 W into 4 Ω and <0.01% THD+N to Clipping
  - 60 dB PSRR (BTL, No Input Signal)
  - <60 µV (A-Weighted) Output Noise
  - >111 dB (A Weighted) SNR
- Multiple Configurations Possible:
  - Stereo, Mono, 2.1 and 4xSE
- Click and Pop Free Startup and Stop
- 90% Efficient Class-D Operation (4 Ω)
- Wide 12-V to 36-V Supply Voltage Operation
- Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short Circuit Protection) With Error Reporting
- EMI Compliant When Used With Recommended System Design

2 Applications

- Blu-ray Disk™ / DVD Receivers
- High End HTiB Systems
- AV Receivers
- High End Soundbar
- Mini Combo Systems
- Active Speakers and Subwoofers

3 Description

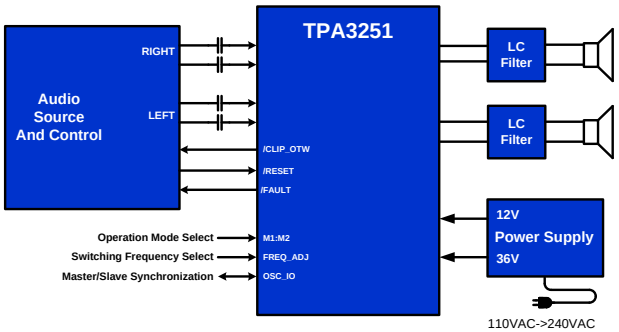
TPA3251 is a high performance class-D power amplifier that enables true premium sound quality with class-D efficiency. It features an advanced integrated feedback design and proprietary high-speed gate driver error correction (PurePath™ Ultra-HD). This technology allows ultra low distortion across the audio band and superior audio quality. The device can drive up to 2 x 175 W into 4-Ω load and 2 x 220 W into 3-Ω load and features a 2 VRMS analog input interface that works seamlessly with high performance DACs such as TI's PCM5242. In addition to excellent audio performance, TPA3251 achieves both high power efficiency and very low power stage idle losses below 1 W. This is achieved through the use of 60 mΩ MOSFETs and an optimized gate driver scheme that achieves significantly lower idle losses than typical discrete implementations.

Device Information(1)

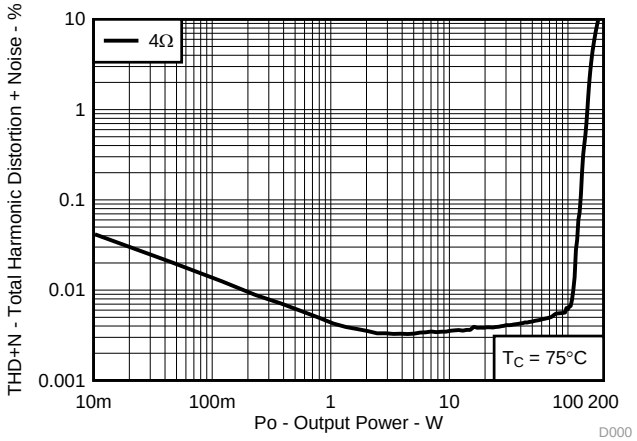
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA3251	HTSSOP (44)	6.10mm x 14.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Total Harmonic Distortion



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2015) to Revision D — **Page**

- Changed the datasheet device number From: TPA3251D2 To TPA3251 ... 1

Changes from Revision B (June 2015) to Revision C — **Page**

- Changed from a one page Product Preview to the full datasheet ... 1

Changes from Revision A (June 2015) to Revision B — **Page**

- Changed *Features* list item From: *80 dB PSRR (BTL, No Input Signal)* To: *60 dB PSRR (BTL, No Input Signal* ... 1
- Changed *Features* list item From: *>112 dB (A Weighted) SNR* To: *>111 dB (A Weighted) SNR* ... 1

Changes from Original (May 2015) to Revision A — **Page**

- Changed the *Features* list for *Total Output Power at 1%THD+N* ... 1
- Changed the *Features* list item *Advanced Integrated Feedback Design...* ... 1
- Changed the *Features* list item From: *<65 µV (A-Weighted) Output Noise* To: *<60 µV (A-Weighted) Output Noise* ... 1
- Changed the *Features* list for *Multiple Configurations Possible:* ... 1
- Changed the *Description* ... 1
- Added the *Simplified Schematic* ... 1

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5 Device Comparison Table

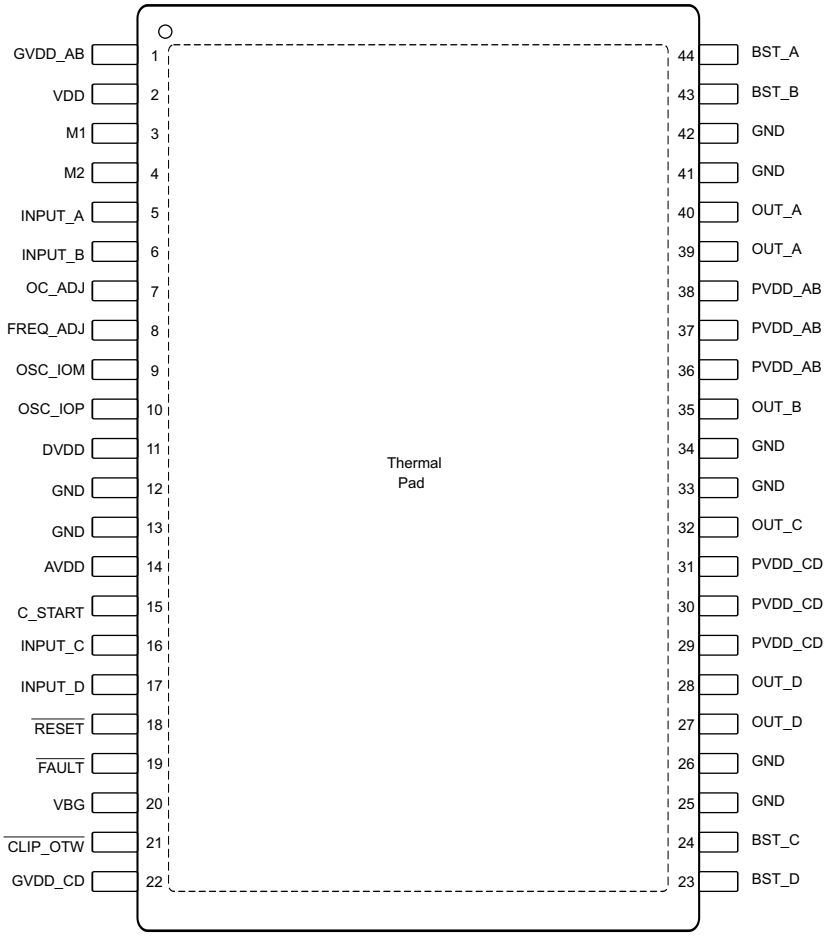
DEVICE NAME	DESCRIPTION
TAS5630B	300-W Stereo Class-D PurePath™ HD Analog Input Audio Power Amplifier
TAS5613A	150-W Stereo Class-D PurePath™ HD Analog Input Audio Power Amplifier
TAS5611A	125-W Stereo Class-D PurePath™ HD Analog Input Audio Power Amplifier

6 Pin Configuration and Functions

The TPA3251 is available in a thermally enhanced TSSOP package.

The package type contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heat sink.

DDV Package
HTSSOP 44-Pin
(Top View)



Pin Functions

NAME	NO.	I/O(1)	DESCRIPTION
AVDD	14	P	Internal voltage regulator, analog section
BST_A	44	P	HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_A required.
BST_B	43	P	HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_B required.
BST_C	24	P	HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_C required.
BST_D	23	P	HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_D required.
$\overline{\text{CLIP\_OTW}}$	21	O	Clipping warning and Over-temperature warning; open drain; active low
C_START	15	O	Startup ramp, requires a charging capacitor to GND
DVDD	11	P	Internal voltage regulator, digital section
$\overline{\text{FAULT}}$	19	O	Shutdown signal, open drain; active low
FREQ_ADJ	8	O	Oscillator freqency programming pin
GND	12, 13, 25, 26, 33, 34, 41, 42	P	Ground
GVDD_AB	1	P	Gate-drive voltage supply; AB-side, requires 0.1 µF capacitor to GND
GVDD_CD	22	P	Gate-drive voltage supply; CD-side, requires 0.1 µF capacitor to GND
INPUT_A	5	I	Input signal for half bridge A
INPUT_B	6	I	Input signal for half bridge B
INPUT_C	16	I	Input signal for half bridge C
INPUT_D	17	I	Input signal for half bridge D
M1	3	I	Mode selection 1 (LSB)
M2	4	I	Mode selection 2 (MSB)
OC_ADJ	7	I/O	Over-Current threshold programming pin
OSC_IOM	9	I/O	Oscillator synchronization interface
OSC_IOP	10	O	Oscillator synchronization interface
OUT_A	39, 40	O	Output, half bridge A
OUT_B	35	O	Output, half bridge B
OUT_C	32	O	Output, half bridge C
OUT_D	27, 28	O	Output, half bridge D
PVDD_AB	36, 37, 38	P	PVDD supply for half-bridge A and B
PVDD_CD	29, 30, 31	P	PVDD supply for half-bridge C and D
$\overline{\text{RESET}}$	18	I	Device reset Input; active low
VDD	2	P	Power supply for internal voltage regulator requires a 10-µF capacitor with a 0.1-µF capacitor to GND for decoupling.
VBG	20	P	Internal voltage reference requires a 0.1-µF capacitor to GND for decoupling.
PowerPad™		P	Ground, connect to grounded heat sink

(1) I=Input, O=Output, I/O= Input/Output, P=Power

Table 1. Mode Selection Pins

MODE PINS		INPUT MODE(1)	OUTPUT CONFIGURATION	DESCRIPTION
M2	M1			
0	0	2N + 1	2 × BTL	Stereo BTL output configuration
0	1	2N/1N + 1	1 x BTL + 2 x SE	2.1 BTL + SE mode
1	0	2N + 1	1 x PBTL	Parallelled BTL configuration. Connect INPUT_C and INPUT_D to GND.
1	1	1N +1	4 x SE	Single ended output configuration

(1) 2N refers to differential input signal, 1N refers to single ended inpout signal. +1 refers to number of logic control (RESET) input pins.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	BST_X to GVDD_X(2)	–0.3	50	V
	VDD to GND	–0.3	13.2	V
	GVDD_X to GND(2)	–0.3	13.2	V
	PVDD_X to GND(2)	–0.3	50	V
	DVDD to GND	–0.3	4.2	V
	AVDD to GND	–0.3	8.5	V
	VBG to GND	-0.3	4.2	V
Interface pins	OUT_X to GND(2)	–0.3	50	V
	BST_X to GND(2)	–0.3	62.5	V
	OC_ADJ, M1, M2, OSC_IOP, OSC_IOM, FREQ_ADJ, C_START, to GND	–0.3	4.2	V
	$\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, $\overline{\text{CLIP\_OTW}}$, $\overline{\text{CLIP}}$ to GND	–0.3	4.2	V
	INPUT_X to GND	–0.3	7	V
	Continuous sink current, $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, $\overline{\text{CLIP\_OTW}}$, $\overline{\text{CLIP}}$, $\overline{\text{RESET}}$ to GND		9	mA
T_J	Operating junction temperature range	0	150	°C
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	12	36	38	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R_L(BTL)	Load impedance	Output filter inductance within recommended value range	2.7	4		Ω
R_L(SE)			1.5	3		
R_L(PBTL)			1.6	2		
L_{OUT}(BTL)	Output filter inductance	Minimum output inductance at I_{OC}	5			μH
L_{OUT}(SE)			5			
L_{OUT}(PBTL)			5			
F_{PWM}	PWM frame rate selectable for AM interference avoidance; 1% Resistor tolerance	Nominal	575	600	625	kHz
		AM1	475	500	525	
		AM2	430	450	470	
$R_{(FREQ\_ADJ)}$	PWM frame rate programming resistor	Nominal; Master mode	9.9	10	10.1	kΩ
		AM1; Master mode	19.8	20	20.2	
		AM2; Master mode	29.7	30	30.3	
C_{PVDD}	PVDD close decoupling capacitors			1.0		μF
R_{OC}	Over-current programming resistor	Resistor tolerance = 5%	22		30	kΩ
$R_{OC(LATCHED)}$	Over-current programming resistor	Resistor tolerance = 5%	47		64	kΩ
$V_{(FREQ\_ADJ)}$	Voltage on FREQ_ADJ pin for slave mode operation	Slave mode		3.3		V
T_J	Junction temperature		0		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPA3251D2 DDV 44-PINS HTSSOP		UNIT
		JEDEC STANDARD 4 LAYER PCB	FIXED 85°C HEATSINK TEMPERATURE(2)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.7	2.5(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.36	0.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	24.4	n/a	
ψ_{JT}	Junction-to-top characterization parameter	0.19	0.5	
ψ_{JB}	Junction-to-board characterization parameter	24.2	n/a	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal data are obtained with 85°C heat sink temperature using thermal compound with 0.7W/mK thermal conductivity and 2mil thickness. In this model heat sink temperature is considered to be the ambient temperature and only path for dissipation is to the heatsink.

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7.5 Electrical Characteristics

PVDD_X = 36 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 600 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
DVDD	Voltage regulator, only used as reference node	VDD = 12 V	3	3.3	3.6	V
AVDD	Voltage regulator, only used as reference node	VDD = 12 V		7.8		V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		40		mA
		Idle, reset mode		13		
I_{GVDD_X}	Gate-supply current per full-bridge	50% duty cycle		25		mA
		Reset mode		3		
I_{PVDD_X}	PVDD idle current per full bridge	50% duty cycle with recommended output filter		12.5		mA
		Reset mode, No switching		1		mA
ANALOG INPUTS						
R_{IN}	Input resistance			24		kΩ
V_{IN}	Maximum input voltage swing				7	V
I_{IN}	Maximum input current				1	mA
G	Inverting voltage Gain	V_{OUT}/V_{IN}		20		dB
OSCILLATOR						
$f_{OSC(IO+)}$	Nominal, Master Mode	F_{PWM} × 6	3.45	3.6	3.75	MHz
	AM1, Master Mode		2.85	3	3.15	
	AM2, Master Mode		2.58	2.7	2.82	
V_{IH}	High level input voltage		1.86			V
V_{IL}	Low level input voltage				1.45	V
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low side (LS)	T_J = 25°C, Includes metallization resistance, GVDD = 12 V		60	100	mΩ
	Drain-to-source resistance, high side (HS)			60	100	mΩ
I/O PROTECTION						
$V_{uvp,VDD,GVDD}$	Undervoltage protection limit, GVDD_x and VDD			9.5		V
$V_{uvp,VDD,\ GVDD,hyst}$ (1)				0.6		V
OTW	Overtemperature warning, $\overline{\text{CLIP\_OTW}}$ (1)		115	125	135	°C
OTW_{hyst} (1)	Temperature drop needed below OTW temperature for $\overline{\text{CLIP\_OTW}}$ to be inactive after OTW event.			25		°C
OTE (1)	Overtemperature error		145	155	165	°C
OTE-$OTW_{(differential)}$ (1)	OTE-OTW differential			30		°C
OTE_{hyst} (1)	A reset needs to occur for $\overline{\text{FAULT}}$ to be released following an OTE event			25		°C
OLPC	Overload protection counter	f_{PWM} = 600 kHz		1.7		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 22 kΩ		14		A
$I_{OC(LATCHED)}$	Overcurrent limit protection	Resistor – programmable, peak current in 1Ω load, R_{OCP} = 47kΩ		14		A
I_{DCspkr}	DC Speaker Protection Current Threshold	BTL current imbalance threshold		1.5		A
I_{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent.		150		ns
I_{PD}	Output pulldown current of each half	Connected when $\overline{\text{RESET}}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA

(1) Specified by design.

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Electrical Characteristics (continued)

PVDD_X = 36 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 600 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	M1, M2, OSC_IOP, OSC_IOM, RESET	1.9			V
V_{IL}	Low level input voltage				0.8	V
I_{lkg}	Input leakage current				100	µA
OTW/SHUTDOWN (FAULT)						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{CLIP\_OTW}}$ to DVDD, $\overline{\text{FAULT}}$ to DVDD		20	26	32	kΩ
V_{OH}	High level output voltage	Internal pullup resistor	3	3.3	3.6	V
V_{OL}	Low level output voltage	I_O = 4 mA		200	500	mV
Device fanout	$\overline{\text{CLIP\_OTW}}$, $\overline{\text{FAULT}}$	No external pullup		30		devices

7.6 Audio Characteristics (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N		220		W
		R_L = 4 Ω, 10% THD+N		175		
		R_L = 3 Ω, 1% THD+N		175		
		R_L = 4 Ω, 1% THD+N		140		
THD+N	Total harmonic distortion + noise	1 W		0.005%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		60		µV
$\lvert V_{OS} \rvert$	Output offset voltage	Inputs AC coupled to GND		20	60	mV
SNR	Signal-to-noise ratio (1)			111		dB
DNR	Dynamic range			115		dB
P_{idle}	Power dissipation due to Idle losses (I_{PVDD_X})	P_O = 0, 4 channels switching (2)		1		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

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7.7 Audio Characteristics (SE)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 2 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 µH, C_{DEM} = 1 µF, MODE = 11, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N		84		W
		R_L = 3 Ω, 10% THD+N		60		
		R_L = 4 Ω, 10% THD+N		47		
		R_L = 2 Ω, 1% THD+N		67		
		R_L = 3 Ω, 1% THD+N		48		
		R_L = 4 Ω, 1% THD+N		37		
THD+N	Total harmonic distortion + noise	1 W		0.015%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		115		µV
SNR	Signal to noise ratio(1)	A-weighted		100		dB
DNR	Dynamic range	A-weighted		101		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		0.5		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

7.8 Audio Characteristics (PBTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 2 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, MODE = 10, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N		355		W
		R_L = 3 Ω, 10% THD+N		250		
		R_L = 4 Ω, 10% THD+N		195		
		R_L = 2 Ω, 1% THD+N		285		
		R_L = 3 Ω, 1% THD+N		200		
		R_L = 4 Ω, 1% THD+N		155		
THD+N	Total harmonic distortion + noise	1 W		0.05%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		62		µV
SNR	Signal to noise ratio(1)	A-weighted		111		dB
DNR	Dynamic range	A-weighted		111		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		1		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

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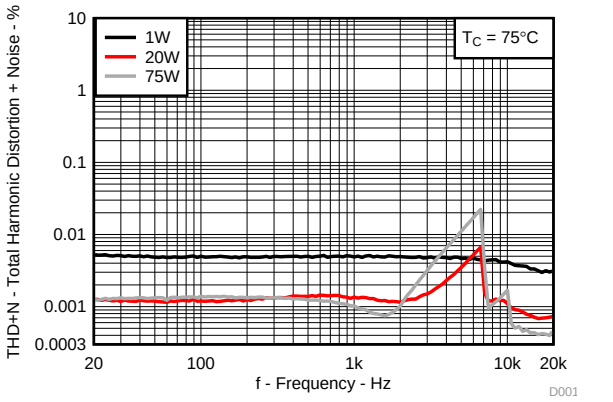
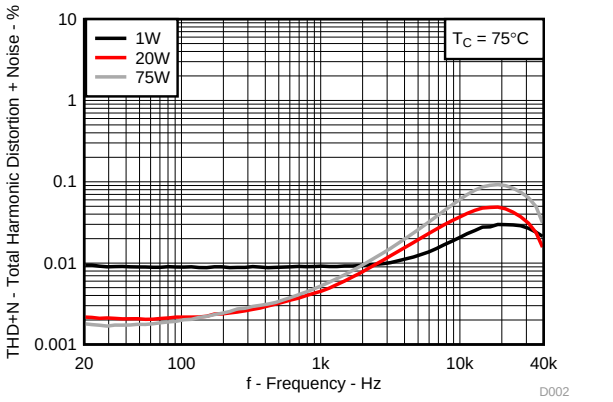
7.9 Typical Characteristics, BTL Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.



R_L = 4 Ω P = 1W, 20W, 75W T_C = 75°C

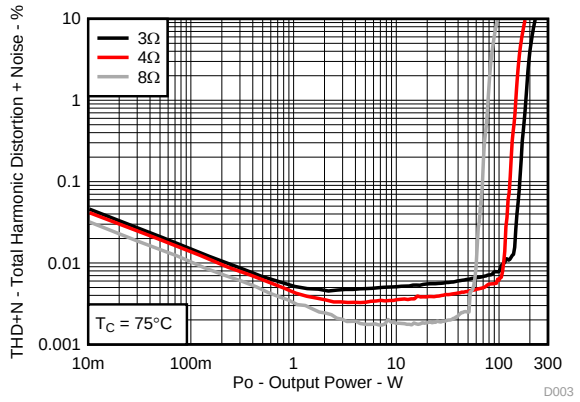
Figure 1. Total Harmonic Distortion+Noise vs Frequency



R_L = 4 Ω P = 1W, 20W, 75W T_C = 75°C

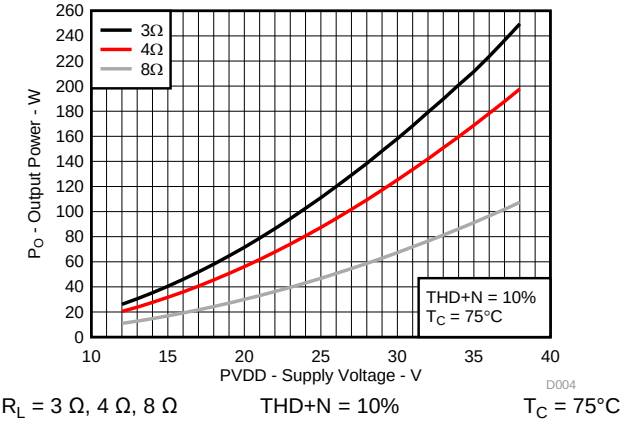
AUX-0025 filter, 80 kHz analyzer BW

Figure 2. Total Harmonic Distortion+Noise vs Frequency



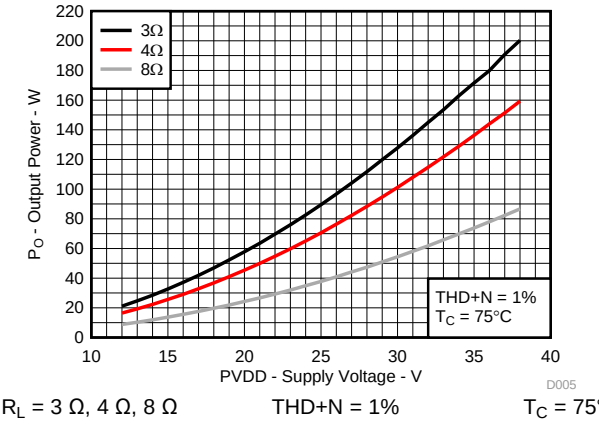
R_L = 3 Ω, 4 Ω, 8 Ω T_C = 75°C

Figure 3. Total Harmonic Distortion + Noise vs Output Power



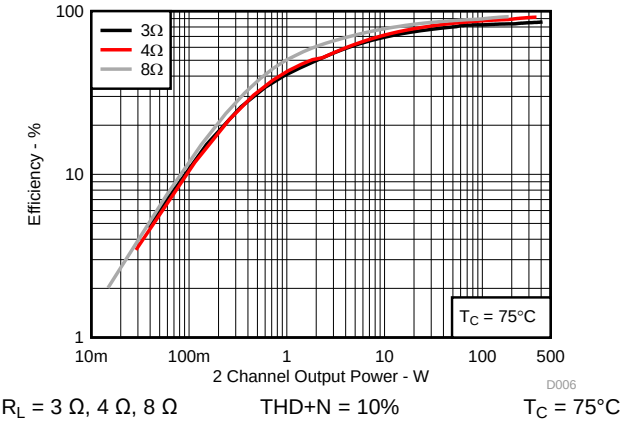
R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 4. Output Power vs Supply Voltage



R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 1% T_C = 75°C

Figure 5. Output Power vs Supply Voltage



R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 6. System Efficiency vs Output Power

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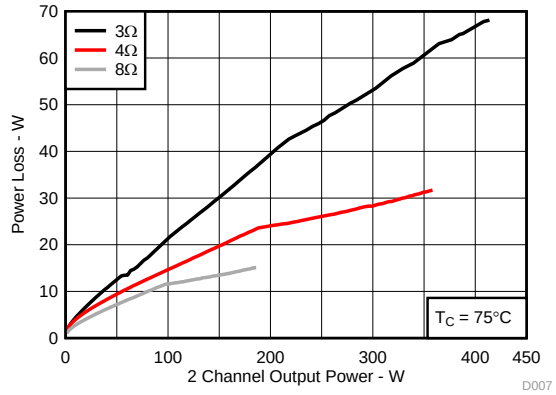
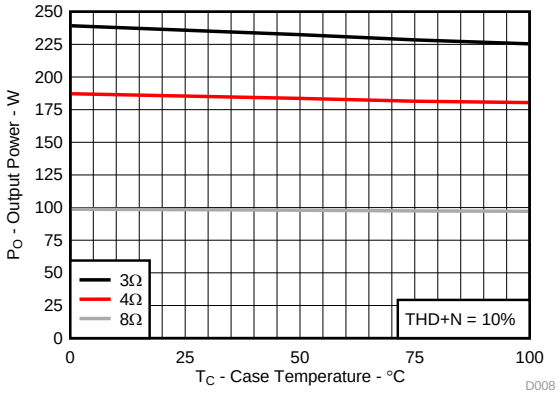
Typical Characteristics, BTL Configuration (continued)

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.



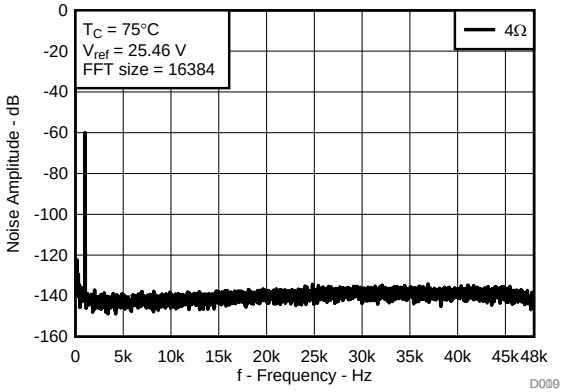
R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 7. System Power Loss vs Output Power



R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 8. Output Power vs Case Temperature

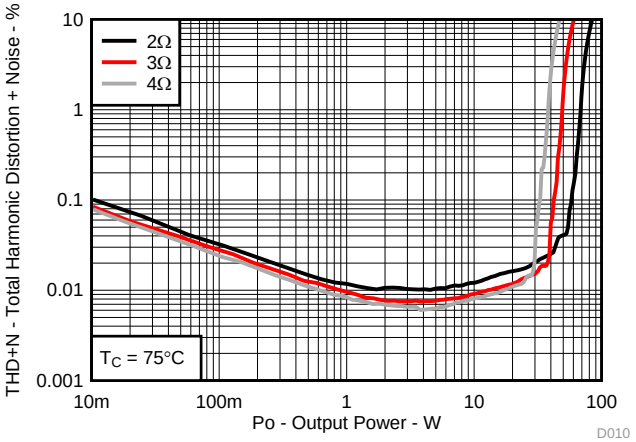


4 Ω, V_{REF} = 25.46 V (1% Output power) FFT = 16384
AUX-0025 filter, 80 kHz analyzer BW T_C = 75°C

Figure 9. Noise Amplitude vs Frequency

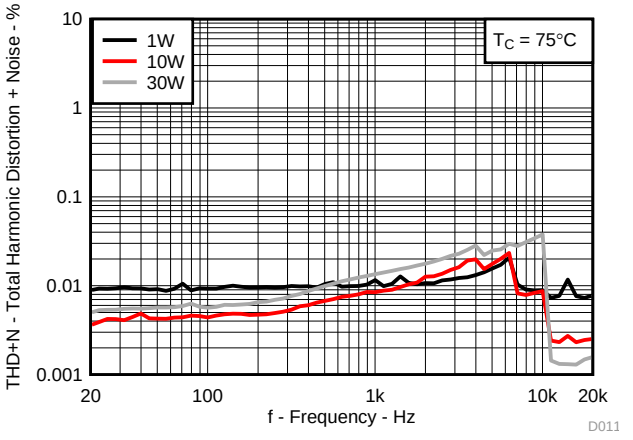
7.10 Typical Characteristics, SE Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 3 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 µH, C_{DEM} = 680 nF, MODE = 11, AES17 + AUX-0025 measurement filters, unless otherwise noted.



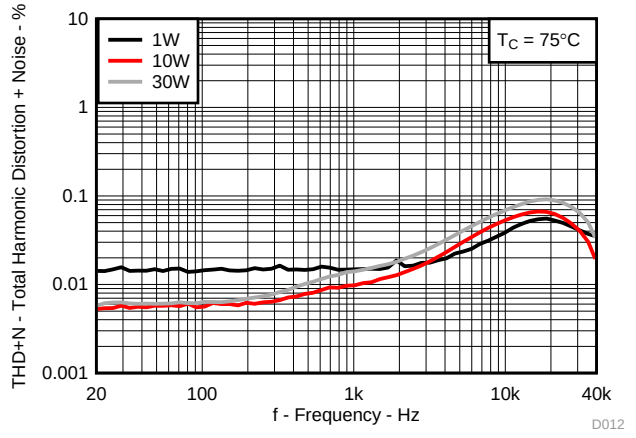
R_L = 2Ω, 3Ω, 4Ω T_C = 75°C

Figure 10. Total Harmonic Distortion+Noise vs Output Power



R_L = 3Ω P = 1W, 10W, 30W T_C = 75°C

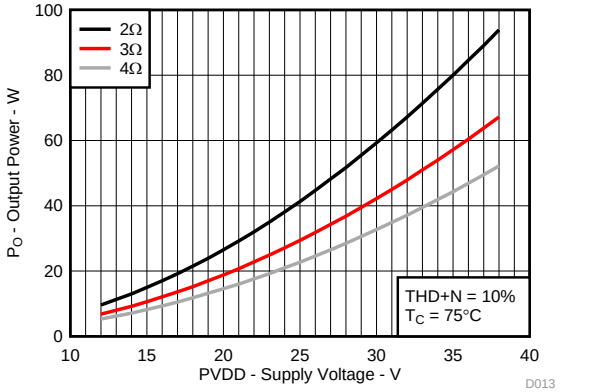
Figure 11. Total Harmonic Distortion+Noise vs Frequency



R_L = 3Ω P = 1W, 10W, 30W T_C = 75°C

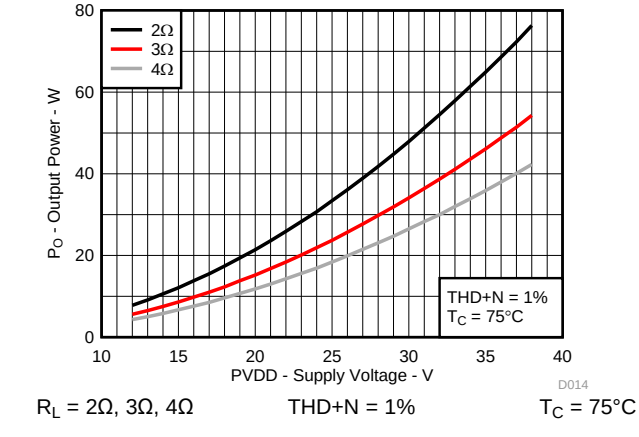
AUX-0025 filter, 80 kHz analyzer BW

Figure 12. Total Harmonic Distortion+Noise vs Frequency



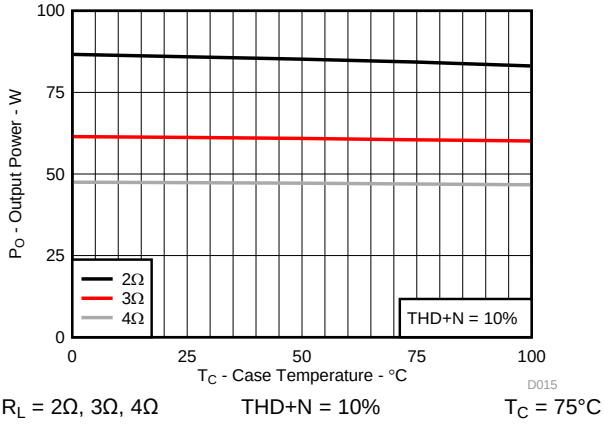
R_L = 2Ω, 3Ω, 4Ω THD+N = 10% T_C = 75°C

Figure 13. Output Power vs Supply Voltage



R_L = 2Ω, 3Ω, 4Ω THD+N = 1% T_C = 75°C

Figure 14. Output Power vs Supply Voltage



R_L = 2Ω, 3Ω, 4Ω THD+N = 10% T_C = 75°C

Figure 15. Output Power vs Case Temperature

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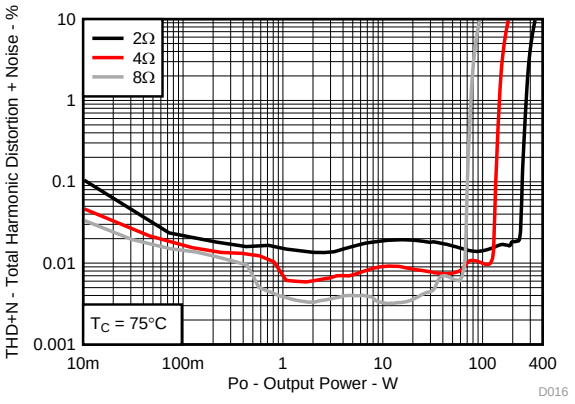
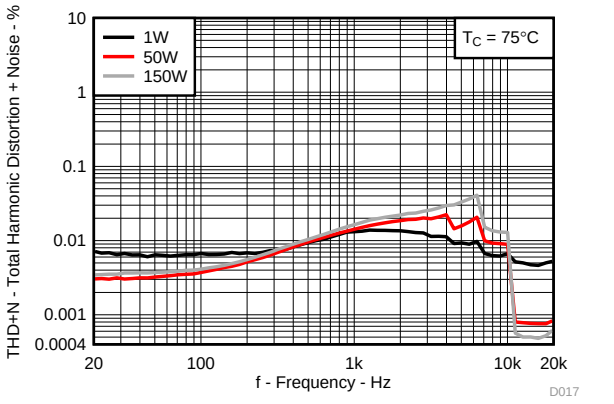
7.11 Typical Characteristics, PBTL Configuration

All Measurements taken at audio frequency = 1kHz, PVDD_X = 36V, GVDD_X = 12V, R_L = 2Ω, f_S = 600 kHz, R_{OC} = 22kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10µH, C_{DEM} = 1 µF, MODE = 10, AES17 + AUX-0025 measurement filters, unless otherwise noted.



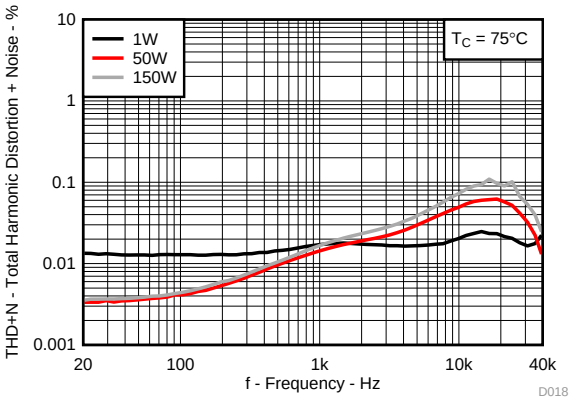
R_L = 2Ω, 4Ω, 8Ω T_C = 75°C

Figure 16. Total Harmonic Distortion+Noise vs Output Power



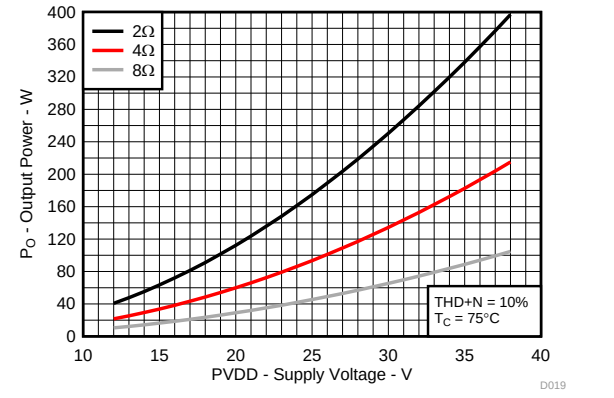
R_L = 2Ω P = 1W, 50W, 1.50W T_C = 75°C

Figure 17. Total Harmonic Distortion+Noise vs Frequency



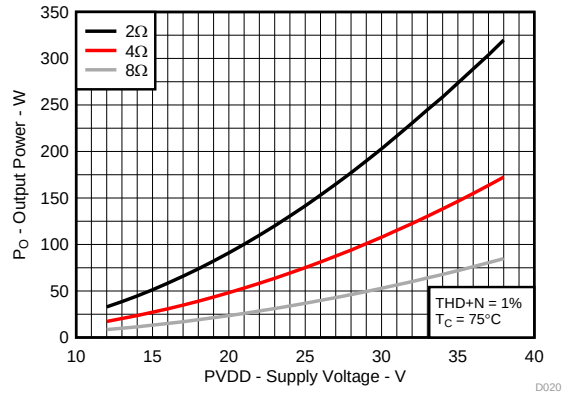
R_L = 2Ω P = 1W, 50W, 150W T_C = 75°C
AUX-0025 filter, 80 kHz analyzer BW

Figure 18. Total Harmonic Distortion+Noise vs Frequency



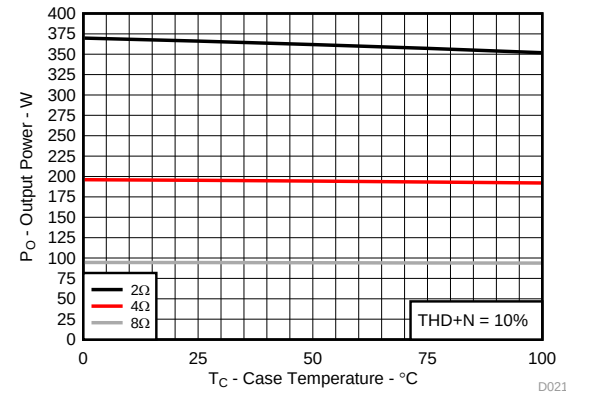
R_L = 2Ω, 4Ω, 8Ω THD+N = 10% T_C = 75°C

Figure 19. Output Power vs Supply Voltage



R_L = 2Ω, 4Ω, 8Ω THD+N = 1% T_C = 75°C

Figure 20. Output Power vs Supply Voltage



R_L = 2Ω, 4Ω, 8Ω THD+N = 10% T_C = 75°C

Figure 21. Output Power vs Case Temperature

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Recommended Operating Conditions*, *Typical Characteristics, BTL Configuration*, *Typical Characteristics, SE Configuration* and *Typical Characteristics, PBTL Configuration* sections.

Most audio analyzers will not give correct readings of Class-D amplifiers' performance due to their sensitivity to out of band noise present at the amplifier output. AES-17 + AUX-0025 pre-analyzer filters are recommended to use for Class-D amplifier measurements. In absence of such filters, a 30-kHz low-pass filter (10 Ω + 47 nF) can be used to reduce the out of band noise remaining on the amplifier outputs.

9 Detailed Description

9.1 Overview

To facilitate system design, the TPA3251 needs only a 12-V supply in addition to the (typical) 36-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry, AVDD and DVDD. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

The audio signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X). Power-stage supply pins (PVDD_X) and gate drive supply pins (GVDD_X) are separate for each full bridge. Although supplied from the same 12-V source, separating to GVDD_AB, GVDD_CD, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details) is recommended. These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see reference board documentation for additional information).

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. It is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each full-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X node is decoupled with 1-µF ceramic capacitor placed as close as possible to the supply pins. It is recommended to follow the PCB layout of the TPA3251 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 36-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit, but it is recommended to release $\overline{\text{RESET}}$ after the power supply is settled for minimum turn on audible artefacts. Moreover, the TPA3251 is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the *Recommended Operating Conditions* table of this data sheet).

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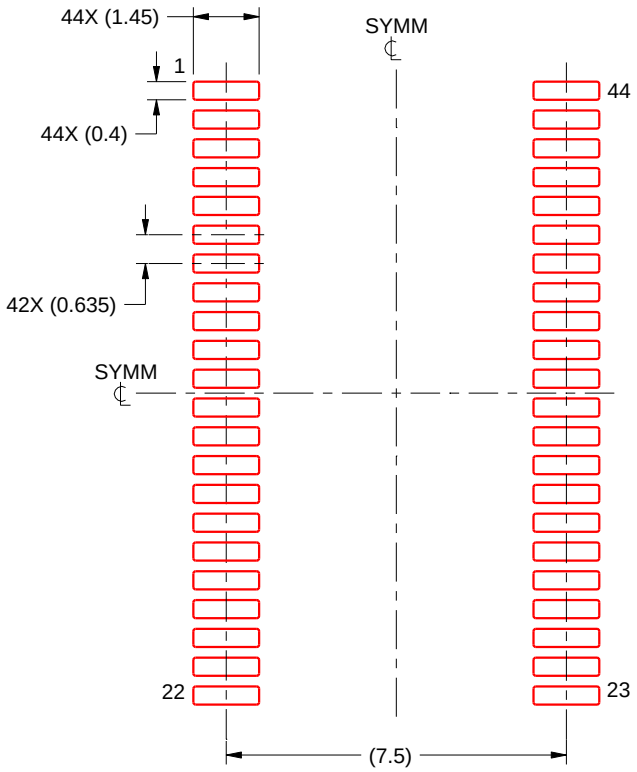

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE :6X

4218830/A 08/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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